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BiSS® C-mode (unidirectional) for RESOLUTE™ and FORTiS™ encoders

About Renishaw encoders with BiSS interface

Renishaw BiSS encoders have options to use the C-mode (unidirectional) BiSS serial interface, (**www.renishaw.com/biss-protocol-support**).

- RESOLUTE rotary encoders are single-turn (with 2^n counts per revolution and no revolution counting).
- RESOLUTE and FORTiS linear encoders are available with a range of different resolutions (and maximum measuring lengths) as specified on the product data sheet.

More information on BiSS serial interfaces is available on the BiSS website: **www.biss-interface.com**.

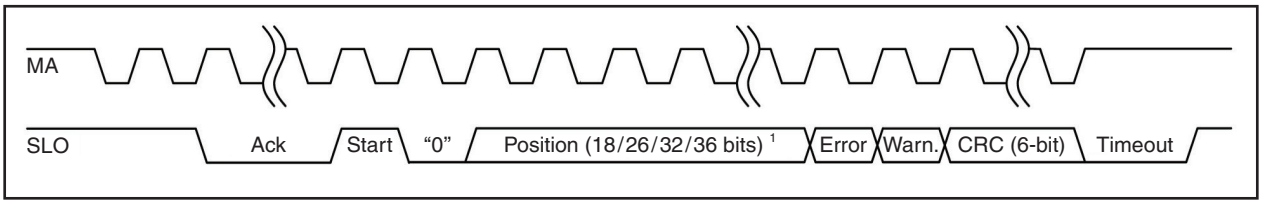
Description of the BiSS interface

BiSS C-mode (unidirectional) is a fast synchronous serial interface for acquiring position data from an encoder. It is a master-slave interface. The master controls the timing of position acquisition and the data transmission speed, and the encoder is the slave. The interface consists of two unidirectional differential pairs of lines:

- MA transmits position acquisition requests and timing information (clock) from master to encoder.
- SLO transfers position data from encoder to master, synchronised to MA.

The diagram below shows the data transmitted.

Data format



The master-slave signal communication format is RS485/RS422 differential line-driven.

[1] For limitations on position word length on FORTiS encoders, please see "Position" under the section headed "Description of data".

A typical request cycle proceeds as follows:

1. When idle, the master holds MA high. The encoder indicates it is ready by holding SLO high.
2. The master requests position acquisition by starting to transmit clock pulses on MA.
3. The encoder responds by setting SLO low on the second rising edge on MA.
4. After the Ack period is complete, the encoder transmits data to the master synchronised with the clock as shown above.
5. When all data has been transferred, the master stops the clock and sets MA high.
6. If the encoder is not yet ready for the next request cycle, it sets SLO low (the Timeout period).
7. When the encoder is ready for the next request cycle, it indicates this to the master by setting SLO high.

Description of data

Ack

This is the period during which the readhead calculates the absolute position. See the timing information table on the next page.

Start and “0” (1 bit each)

The encoder transmits the start bit to signal to the master that it is starting to transmit data. The start bit is always high and the “0” bit is always low.

Position (18, 26, 32 or 36 bits)

The absolute position data is sent MSB first in binary format. For rotary encoders, there are exactly 2^n counts per revolution, after which the count “wraps around” to zero. Lower resolutions may be achieved by ignoring the least significant bit(s) of the position data.

For FORTiS encoders, the standard position word length is 36 bits and this should be used whenever possible. For special requirements, 26 bit word length is available with 50 nm resolution, and 32 bit word length is available with 10 nm resolution.

Error (1 bit)

The error bit is active low: “1” indicates that the transmitted position information has been verified by the readhead’s internal safety checking algorithm and is correct; “0” indicates that the internal check has failed and the position information should not be trusted. The error bit is also set to “0” if the temperature exceeds the maximum specified for the product. The operating temperature limits of RESOLUTE and FORTiS systems are specified in the product data sheets.

Warning (1 bit)

The warning bit is active low: “0” indicates that the encoder scale (and / or reading window) should be cleaned.

NOTE: The warning bit is not an indication of the trustworthiness of the position data. Only the error bit should be used for this purpose.

CRC for position data (6 bit)

The CRC polynomial for position, error and warning data is: $x^6 + x^1 + x^0$. The CRC start value is 0x00. It is transmitted MSB first and inverted. The start bit and “0” bit are omitted from the CRC calculation.

Timeout

RESOLUTE and FORTiS encoders are capable of acquiring a new position reading every 31.25 µs (a maximum request cycle rate of 32 kHz). Therefore 31.25 µs must elapse between the start of one request cycle and the start of the next. However, it is possible for data transmission to be complete before 31.25 µs have elapsed. In this case, the encoder signals this to the master by holding the SLO line low until 31.25 µs have elapsed. This is the timeout period.

Resetting the encoder

The master may reset the encoder at any time during a request cycle by stopping the clock and setting MA high. MA must be held high for the remaining duration of the full request cycle, including timeout period if applicable.

NOTE: SLO may be high or low during resetting (typically depending on the state of the last bit transmitted).

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Line delay compensation

Signals travelling between master and encoder experience a time delay due to the cable length and signal propagation delays within the master and encoder. The time delay has no effect at low clock speeds (where the time delay is much shorter than the clock period). However, for high clock speeds, it is necessary for the master to implement line delay compensation.

The master determines the round-trip time delay by measuring the time between transmitting the second rising edge on MA and receiving the falling edge of “Ack” on SLO.

MA clock speed	Maximum cable length	
	Without line-delay compensation	With line-delay compensation
250 kHz	95 m	100 m
1 MHz	20 m	100 m
2 MHz	8 m	100 m
5 MHz	0.5 m	100 m
10 MHz	-	50 m

NOTES:

- All figures relate to installations using either:
  - RESOLUTE readhead with original Renishaw cable up to 10 m in length, with the remainder cable length consisting of Renishaw approved extension cable or,
  - FORTiS encoder with original Renishaw cables as specified in the ‘Cables for FORTiS™ absolute encoders’ data sheet (Renishaw part no. L-9517-0069).
- Care should be taken to ensure supply voltage is maintained within 5 V ±10% at the readhead connector. For FORTiS encoders, the restrictions detailed in the section “Maximum cable lengths” in the ‘Cables for FORTiS™ absolute encoders’ data sheet (Renishaw part no. L-9517-0069) must be followed.
- This table makes no allowance for propagation delays within the master.

Timing information

	Minimum	Typical	Maximum	Units	Notes
Ack time	-	-	16	µs	The Ack period always ends on a rising edge of MA. Therefore at low MA clock frequencies, the Ack time may exceed 16 µs.
MA clock frequency	0.25	-	10	MHz	Within any one request cycle, the MA clock frequency must be constant. The duty cycle should be 1:1.
Request cycle rate	-	-	32	kHz	32 kHz is not achievable for all MA clock frequencies (because data transmission takes too long).
Sampling moment	3.225	3.250	3.275	µs	Timed from the first rising edge on MA.
RESOLUTE/FORTiS internal line-delay	-	-	42.5	ns	This is the internal propagation delay (MA-SLO) within RESOLUTE and FORTiS encoders.
Line-delay due to cable length	-	10	-	ns/m	This is the round-trip delay experienced by signal travelling through the cable (that is, from master to encoder and back to master again).

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