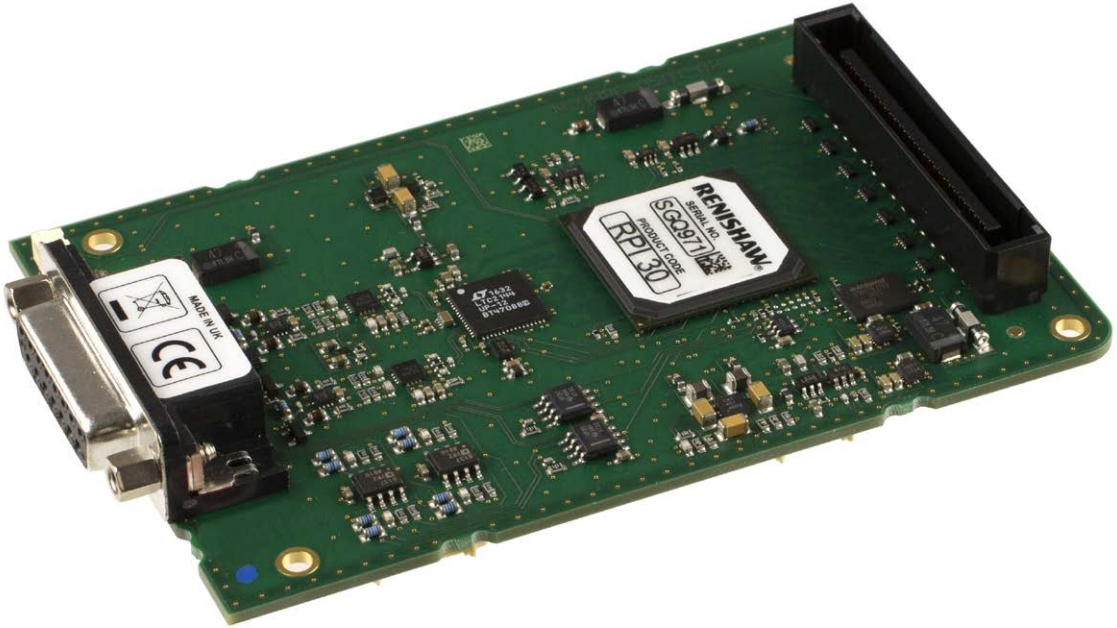
User's guide
F-9926-0018-01-B

RPI30 parallel interface



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Care of equipment

The RPI30 parallel interface contains precision electronic components. Avoid exposure to moisture. Remove power before connecting, disconnecting, handling or changing switch settings.

WARNING: Use correct handling techniques when touching any of the RPI30 assemblies to prevent damage from electrostatic discharge (ESD).

Changes to Renishaw products

Renishaw plc reserves the right to improve, change or modify its products and documentation without incurring any obligation to make changes to Renishaw equipment previously sold or distributed.

Warranty

Renishaw plc warrants its equipment provided that it is installed exactly as defined in associated Renishaw documentation.

Renishaw part no: F-9926-0018-01-B
Issued: 05 2020

Safety

It is the responsibility of the manufacturer and/or encoder system installation authority to ensure that, in safety critical applications of the RPI30 parallel interface, any form of signal deviation from the limits of the receiving electronics, howsoever caused, shall not cause the machine to become unsafe. It is also their responsibility to ensure that the end user is made aware of any hazards involved in the operation of their machine, including those mentioned in Renishaw product documentation, and to ensure that adequate guards and safety interlocks are provided.

When using the RPI30 as part of a positioning system on machines, beware of pinch and/or crush hazards that can be created, depending on how and where the equipment is installed.

Further information on safety is contained in Appendix B.

The RPI30 has been designed for use with an RLE laser encoder only. Its use is not supported with other encoder systems.

FCC notice

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

The user is cautioned that any changes or modifications not expressly approved by Renishaw plc or authorised representative could void the user's authority to operate the equipment.

EC compliance

CE

Renishaw plc declares that the RPI30 parallel interface complies with the applicable directives, standards and regulations. A copy of the full EC Declaration of Conformity is available at the following address:

www.renishaw.com/RLECE

WEEE

The use of this symbol on Renishaw products and/or accompanying documentation indicates that the product should not be mixed with general household waste upon disposal. It is the responsibility of the end user to dispose of this product at a designated collection point for waste electrical and electronic equipment (WEEE) to enable reuse or recycling. Correct disposal of this product will help to save valuable resources and prevent potential negative effects on the environment. For more information, please contact your local waste disposal service or Renishaw distributor.

Packing material information

Compliant with EC directive 2011/65/EU (RoHS)

Packaging component	Material	94/62/EC code	94/62/EC number
Metalised bag	Aluminium foil/PETP laminate	C/PET	90
Cartons	Cardboard - 70% recycled content	PAP	20
Bubble bags	Low density polyethylene	LDPE	4

REACH regulation

Information required by Article 33(1) of Regulation (EC) No. 1907/2006 ("REACH") relating to products containing substances of very high concern (SVHCs) is available at:

www.renishaw.com/REACH

RoHS compliance

Compliant with EC directive 2011/65/EU (RoHS)

Contents

1 System overview

The RPI30 converts 1 Vpp analogue quadrature signals from an RLE laser interferometer encoder system into a position reading, which is available over a parallel bus. The RPI30 interface includes active Sub Divisional Error (SDE) correction, to further reduce the effect of errors within the motion control system. This is applied by actively updating the DC offset and AC mismatch when the system is in use to achieve the highest performance.

Additionally the RPI30 has an separate diagnostics connection to allow diagnostics information to be downloaded and analysed remotely.

The RPI30 gives an output of both axis position and status over a LVTTL (3.0 V) compatible bus. The position is available as a 36-bit two's complement word, with a choice of least significant bit (LSB) resolution. The status information includes the signal strength and error flags.

RPI30 fast parallel interface

Part numbers

The following saleable part number is available:

- A-9926-0700 RPI30 fast parallel interface

In addition, the mating half of the RPI30 parallel bus connectors can also be supplied by Renishaw. The saleable part number is:

- A-9904-2256 RPI connector 0°

For information on the connector please refer to Section 2.

2 Installation

2.1 Handling precautions

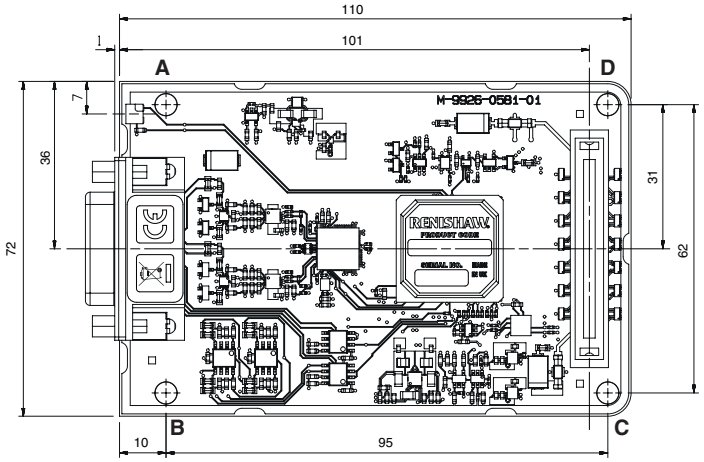
WARNING: Use correct handling techniques when touching any of the RPI30 assemblies to prevent damage from ESD.

2.2 Mounting and fixing

The RPI30 can be supported using the four mounting holes (A, B, C and D) which are suitable for M3 screws. The position of the holes are shown within diagram opposite. All dimensions are in millimetres.

Note: Holes A and B are electrically connected to chassis ground. Holes C and D are unconnected.

Note: Mounting screws should not exceed a maximum torque of 0.6 nm.



RPI30 fast parallel interface dimensions

2.3 Analogue quadrature interface

The RPI30 accepts the nominal 1 Vpp analogue quadrature from the RLE. Signal termination is contained within the RPI30 itself. There is no need for any other termination to be used.

Cabling

The choice of cables for this application is very important. A cable with individually screened twisted pairs is recommended. An example of a suitable cable is the Belden 8164 cable. The maximum recommended cable length is 10 m. The signals should be wired as shown in the table below:

Signal	Function
1st pair	Sine and /Sine
2nd pair	Cosine and /Cosine
3rd pair	Error and /Error
Individual screens	0 V (both ends)
Outer screen	Case/shell (both ends)

Signal wiring between RLE and RPI30

WARNING: It is essential that the error line inputs are connected so that the RPI30 can determine if any errors have occurred in the RLE system. If the analogue quadrature is incorrectly wired, the system may still work but may move distances and at speeds that are not expected and may move in the opposite direction to that expected. If a voltage exceeding ±7 V is applied on any of the signals, damage to the unit can occur.

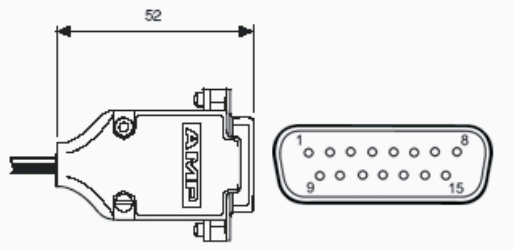
WARNING: Care should be taken to ensure that individual signal wires do not short. It is advised that all joints are sleeved. If input signal wires short, the position output will be unreliable and the error signal may not work reliably.

Connector pin out

The analogue quadrature input connector pin out is shown in the table below. All pins are protected to ±7 V. The connector on the RPI30 is a 15 way female D-type. The diagram opposite shows the mating D-type connector.

Pin number	Function
1	0 V
2	–
3	Error
4	–
5	Sine
6	Cosine
7	–
8	–
9	–
10	/Error
11	–
12	/Sine
13	/Cosine
14	–
15	–
Shell	Chassis ground

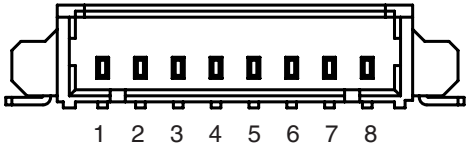
Analogue quadrature input (15 way D-type male)



Analogue quadrature input mating connector (15 way D-type male connector)

2.4 Analogue feed through

The analogue quadrature and error inputs are buffered and available on an 8-way picoblade connector. These are copies of the input signals and do not have any SDE correction appled or RPI30 errors included. The analogue quadrature signals should be terminated with 120ohm.

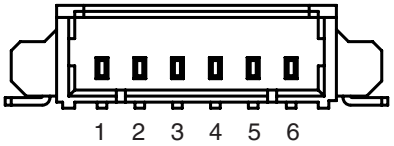


Pin number	Function
1	/Sine
2	Sine
3	0V
4	/Cosine
5	Cosine
6	0V
7	Error
8	/Error

Analogue feedthrough connector (8-way picoblade)

2.5 Diagnostics

A full duplex RS422 UART connection is provided to access the diagnostic and control registers in addition to the normal SPI interface. Full details can be found in Appendix D.



Pin number	Function
1	Rx +
2	Rx -
3	0v
4	0v
5	Tx +
6	Tx -

Diagnostics connector (6-way picobade)

2.6 Parallel interface

Connector

The correct mating connectors for the RPI30 parallel bus are the JAE TX24 60R family of connectors. These may be supplied by Renishaw or direct from JAE.

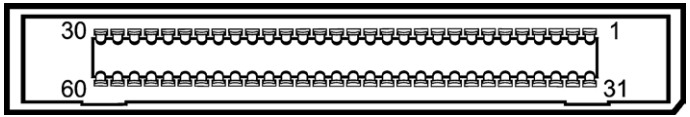
Pin	Label	Pin	Label	Pin	Label	Pin	Label
1	5 V	16	DTA26	31	5 V	46	DTA19
2	0 V	17	DTA25	32	0 V	47	DTA18
3	DTA15	18	DTA24	33	DTA7	48	DTA17
4	DTA14	19	DTA33	34	DTA6	49	DTA16
5	DTA13	20	DTA32	35	DTA5	50	DTA35
6	DTA12	21	DTA34	36	DTA4	51	Reserved
7	DTA11	22	Reserved	37	DTA3	52	Reserved
8	DTA10	23	Reserved	38	DTA2	53	SDI
9	DTA9	24	ADD4	39	DTA1	54	SDO
10	DTA8	25	ADD3	40	DTA0	55	SCLK
11	DTA31	26	ADD2	41	DTA23	56	CSB
12	DTA30	27	ADD1	42	DTA22	57	Reserved
13	DTA29	28	ADD0	43	DTA21	58	/Enable
14	/Error (O/C)	29	0 V	44	DTA20	59	0 V
15	DTA27	30	5 V	45	DTA28	60	5 V

RPI30 parallel bus connector pin out

Description	Renishaw part number	JAE part number
RPI mating 0° connector	A-9904-2256	TX24-60R-6ST-H1E

Part number for JAE connector

Note: using RPI mating 0° connector, A-9904-2256, separation between boards = 12 mm



RPI30 parallel bus mating connector

Other separations can be achieved using other receptacles.

For detailed information on the connectors, please visit the JAE web site at: www.jae-connector.com

3 Configuration

3.1 RLE set-up – dip switches

If the RPI30 is being used with an RLE system, care should be taken setting the RLE configuration switches correctly.

RLE switch number	Status	Details
5	DOWN	Analogue quadrature output
11	DOWN	RLE does not tri-state the quadrature on error
12	UP	Set to UP, unless fine digital quadrature output from the RLE is also required (in addition to the RPI30 parallel output)
13	DOWN	RLE does not latch errors, the RPI30 will latch any errors flagged

RLE dip switch settings

Note: The RLE axis direction reversal switches 6 and 7 only affect the direction of the digital quadrature from the RLE and not the analogue quadrature.

Note: Make sure the parity switch is set in accordance with the RLE manual (M-5225-0568)

Note: The RLE will flag an error when the measurement velocity reaches a level at which the required output rate of the digital quadrature exceeds the digital bandwidth limit of the RLE. The digital bandwidth limit depends on the digital quadrature resolution and maximum output bandwidth selected with the RLE DIP switches. The digital quadrature resolution and the digital output bandwidth should be selected so that the RLE measurement velocity limit is sufficient for the application. It is therefore recommended that fine quadrature is disabled by setting RLE switch number 12 UP.

For further information on the RLE front panel switches refer to the RLE manual (M-5225-0568).

3.2 RPI30 set-up

The settings for the parallel interface and lissajous correction are accessible over the SPI interface and also the diagnostics UART interface. Power on settings are stored on EEPROM and can be updated via either interface.

Setting		Factory default
Parallel bus	Address	1
	Direction	0 – Forward
	Resolution	0 – 38.6 pm
Lissajous correction	Enable	127 – all disabled
	Sample length	1000 – 1 ms
	Min quads	8
	Max quads	5000
	Offset filter length	3 – 14 bit
	AC mismatch filter length	3 – 14 bit
User calibration	Sine / cosine offset	0
	Sine / cosine gain	43690 – x1.33

Factory defaults for settings stored in EEPROM

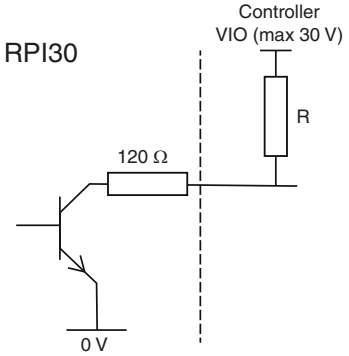
The SPI and UART interfaces also allow access to a variety of additional information including

- RPI30 version
- ADC data
- Position data
- Lissajous correction status
- Independent resetting of errors and position

Full details can be found in Appendix C for the SPI interface and Appendix D for the UART.

3.3 /Error line

The parallel bus includes a /error line which is active low. The /error line indicates if any errors have occurred with either the RLE or the RPI30. The /error line is latched if an error occurs and must be cleared by a reset. The /error line is an open collector output and should be pulled up to the controller IO voltage with a resistor as shown below.



	Maximum
Voltage	30 V
Current	45 mA

/Error maximum ratings

Open collector error output wiring

WARNING: The open collector /error line is not a fail-safe method and therefore additional safety precautions must be taken in safety critical closed loop applications. The /error line must be continually monitored and the motion system must be stopped if it is asserted.

3.4 LED indicator

An LED indicates the status of the RPI30.

LED	Status
Red	RPI30 powered but in error condition
Green	RPI30 powered and no error
Amber	RPI30 powered and in warning state

LED status indicator

4 Communication over the parallel bus

High speed communication with the RPI30 is performed over the parallel bus.

Five functions may be performed over the parallel bus:

1. Latching all of the RPI30 position and status data simultaneously
2. Reading of the latched positions
3. Reading of the latched status information
4. Resetting of the position and clearing of all errors
5. Enabling test information onto the RPI30 parallel bus

All data must be latched before it is read.

4.1 Parallel bus

The parallel bus contains a 5-bit address bus, a 36-bit data bus, /enable line and /error line.

Address bus

The top three lines of the address bus are used to choose which RPI30 unit to communicate with. Each RPI30 unit has a unique base address, selected over the SPI interface, as detailed in Section 3.2. Base address 0 is reserved for simultaneous communication with all RPI30 units on the bus.

The bottom two lines of the address bus are used to define the required function. The address bus functionality is described in the table on page 13.

Data bus

The RPI30 can be requested to put either position or status data on the data bus. The position data is a 36-bit word with DTA0 as the LSB and DTA35 as the MSB. The status information is detailed in the table on page 13.

/Enable

The /enable line has two functions. The first is to latch or reset position and status data. This is initiated by a falling edge of the /enable signal. Secondly, it is used to enable data onto the bus. Refer to table on page 14.

/Error

The /error line indicates when a fault has occurred in the measurement system. It is described in detail in Section 3.3 on page 11.

4.2 Functionality

Five functions may be performed over the parallel bus. These are:

1. Resetting the position and error status of the RPI30
2. Latching the position and status reading of all RPI30s simultaneously
3. Transferring latched position information onto the RPI30 parallel data bus
4. Transferring latched status information onto the RPI30 parallel bus
5. Transferring test information onto the RPI30 parallel bus

The required function is chosen by selecting the correct register. The functionality is shown in the following table.

RPI30	Address location (bit)					Register	Function
	4	3	2	1	0		
All	0	0	0	0	0	1	Latch all RPI30 units
				0	1	2	Reserved
				1	0	3	Reset all RPI30 units
				1	1	4	Reserved
Unit 1	0	0	1	0	0	1	Read RPI30 unit 1 position
				0	1	2	Read RPI30 unit 1 status
				1	0	3	RPI30 unit 1 reset
				1	1	4	Read RPI30 unit 1 test information
Unit 2	0	1	0	0	0	1	Read RPI30 unit 2 position
				0	1	2	Read RPI30 unit 2 status
				1	0	3	RPI30 unit 2 reset
				1	1	4	Read RPI30 unit 2 test information
Unit 7	1	1	1	0	0	1	Read RPI30 unit 7 position
				0	1	2	Read RPI30 unit 7 status
				1	0	3	RPI30 unit 7 reset
				1	1	4	Read RPI30 unit 7 test information

RPI30 address bus functionality

Reset

Register 3 is used to reset the RPI30. If there are no errors currently active in the system, the /error line is reset, any latched error flags are cleared and the position output is set to zero. All RPI30s may be simultaneously reset by addressing register 3 of base address 0 and taking the /enable line low. An individual RPI30 may be reset by addressing register 3 of its base address and taking the /enable line low.

Latch data

Register 1 of base address 0 is used to latch both the position data and the status data of all the RPI30s simultaneously.

Enable position data

Register 1 of a particular RPI30 unit's base address holds the latched position data. If this register is selected on the address bus, then position information is placed on the data bus after the /enable line is taken low. The position output is represented in two's complement format as shown below.

MSN								LSN	Position
7	F	F	F	F	F	F	F	F	$(2^{35}-1 \times UOR)$
0	0	0	0	0	0	0	0	2	2 × UOR
0	0	0	0	0	0	0	0	1	1 × UOR
0	0	0	0	0	0	0	0	0	0 × UOR
F	F	F	F	F	F	F	F	F	-1 × UOR
F	F	F	F	F	F	F	F	F	-2 × UOR
8	0	0	0	0	0	0	0	0	$-2^{35} \times UOR$

Position output in two's complement format

UOR = unit of resolution of LSB as set by control register 4-3
MSN = most significant nibble
LSN = least significant nibble

Enable status data

Register 2 of a particular RPI30 unit holds the latched status information. If this register is selected on the address bus, the status information is placed on the data bus after the /enable line is taken low. Information contained in the status register is detailed in the table below.

Bits	Function	Comment
0-9	Analogue quadrature sample – cosine	This is the digitised input value of the cosine signal *
10-19	Analogue quadrature sample – sine	This is the digitised input value of the sine signal *
20-27	Signal level	Amplitude of input quadrature (0 to FF where FF=115% signal strength) *
28	Encoder error (1 = error)	Error flagged by encoder system
29	Overspeed error (1 = error)	**
30	Beam break error (1 = error)	Input quadrature amplitude too low (<12.5%)
31	Bus setting changed	A setting for the parallel bus has changed.
32-33	Resolution setting	00 = 38.6 pm, 07 = 77.2 pm, 10 = 104.4 pm, 11 = 308.8 pm
34	Direction setting	(0 = FWD, 1 = REV)
35	EEPROM configuration error	Configuration EEPROM CRC failed

Status information

* Bits 0, 10, 20 are the LSBs of the digitised cosine, sine and signal level values respectively.

** An overspeed error is flagged when the input analogue quadrature rate exceeds the processing capability of the RPI30.

Enable test data

Register 4 of a particular RPI30 unit holds test information which can be used for checking the data bus for open and short circuits and failed drivers.

Note: The test information in register 4 may be used to verify the presence of all expected RPI30s at power-up and before engaging drives.

4.3 Timing diagram

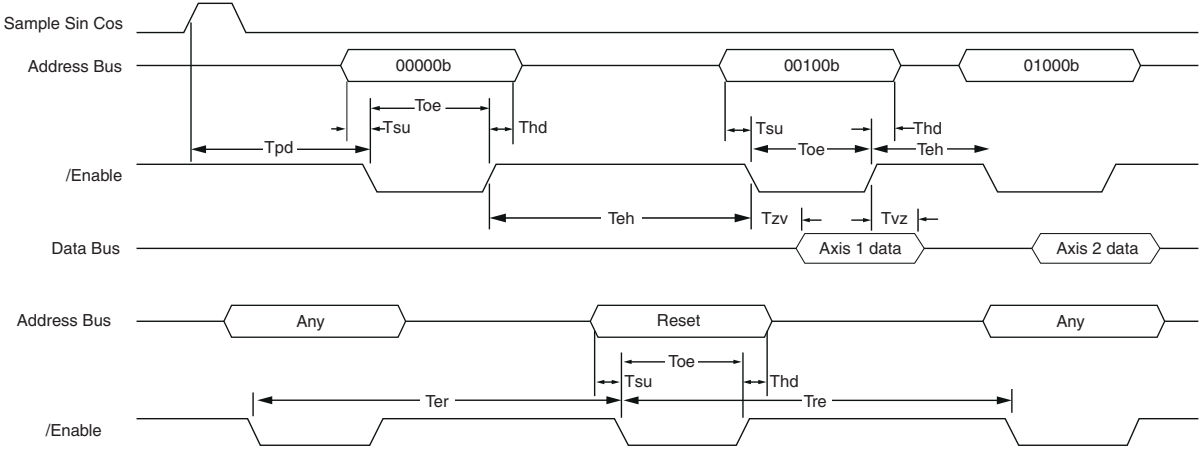
A timing diagram for a two-axis position read is shown below. The read consists of three separate stages.

1. Latch data by asserting /enable with the address but set to 00000b (base address 0, register 1) *
2. Read in position data from axis 1 by taking /enable low whilst the address bus is set to 00100b (base address 1, register 1) **
3. Read in position data from axis 2 by taking /enable low whilst the address bus is set to 01000b (base address 2, register 1) **

The same timing sequence should be used to reset an RPI30.

* This will replace any previously latched data.

** This will not clear the latched position. It can be read again if necessary.



RPI30 parallel bus timing diagram

Parameter	Min	Nom	Max	Units	Comment
Tsu	10			ns	Set-up of address before /Enable falling edge
Toe	50			ns	Minimum period that /Enable must be active
Thd	10			ns	Period address to be held after /Enable rising edge
Tzv			35	ns	/Enable to data valid
Tvz			35	ns	Data valid to hi-impedance state
Tpd	130	135	140	ns	Propagation delay. The time before the /Enable that the position event occurred. This defines the delay due to RPI30 only.
Tsp	100			ns	Time between sequential axis access
Teh	50			ns	Minimum period that /Enable must be high
Ter	100			ns	Minimum delay from /Enable falling edge of previous bus access and reset
Tre	100			ns	Minimum delay between /Enable falling edge of reset and next bus access

Timing parameters

Based on these timings, the maximum update rates for reading the position information depends on the number of axes to be read in sequence, as shown in Appendix A.

Appendix A – Specification

Values in this table define the contribution of the RPI30 on the system performance, NOT the complete laser interferometer system performance.

		PMI	RRI
LSB resolution – user selectable		38.6, 77.2, 154.4 or 308.8 pm	77.2, 154.4 or 308.8, 617.6 pm
Maximum speed		2 m/s	4 m/s
Positional noise contribution (RMS) signal strength >25%		< 38.6 pm	< 77.2 pm
SDE contribution (excluding RLE and without correction enabled)	**Velocity** **< 50 mm/s (PMI)** **< 100 mm/s (RRI)** **Signal strength > 25%**	< ±0.5 nm	< ±1.0 nm
	Velocity **> 50 mm/s and < 1 m/s (PMI)** **> 100 mm/s and < 2 m/s (RRI)**	< ±2 nm	< ±4 nm
SDE including RLE with correction enabled	**Velocity** **< 50 mm/s (PMI)** **< 100 mm/s (RRI)** **Signal strength > 50%**	< ±0.1 nm	< ±0.2 nm
Position data format		36-bit (two's compliment)	
Propagation delay (actual position is sampled) before latch enable signal		135 ns	
Propagation delay variation		±5 ns	
Maximum update rate	**1 axis system**	5 MHz	
	2 axis system	3.3 MHz	

Measurement performance

Voltage	5 V ±0.25 V
Operating current	500 mA
Noise and ripple	50 mVpp (DC to 10 MHz)

RPI30 power requirement

The 5 V power supply should be single fault tolerant certified to EN (IEC) 60950-1.

Pressure	Normal atmospheric (650 mbar – 1150 mbar)	
Humidity	0-95% RH (non-condensing)	
Temperature	Storage	-20 °C to +70 °C
	Operating	+10 °C to +40 °C

Environmental specification

Digital interface on the JAE connector is 3.0 V LVCMOS and it is compatible with 3.3 V LVTTL.

	Min (V)	Max (V)
Input low	-0.3	0.8
Input high	1.7	3.6
Output low	0	0.2
Output high	2.8	3.0

Digital interface voltage specifications

Appendix B – Safety information

General

The RPI30 is designed for integration into the primary position feedback loop of a motion system. It is essential that the system is installed in accordance with the instructions in the installation manuals. It is the responsibility of the system integrator to ensure that, in the event of a failure of any part of the RPI30, the motion system remains safe.

In motion systems with powers or speeds capable of causing injury, safety protection measures must be included in the design. It is recommended that satisfactory operation of these protection measures is verified **before** the feedback loop is closed. The following are examples of safety protection measures that can be used. It is the sole responsibility of the system integrator to select appropriate measures for their application.

1. The RPI30 includes an error signal output. The control system must be designed to stop the axis motion if this error is asserted.
2. The axis must include physical limit switches which, when tripped, will stop axis motion before damage occurs (soft limits alone are insufficient).
3. Motor torque monitoring. If the motor torque exceeds an expected limit, the axis of motion must be stopped.
4. The machine must include an emergency stop button.
5. Following error detection, if the difference between the controller demand position and the axis feedback position exceeds an expected limit, the axis motion must be stopped.
6. Guards, viewing windows, covers and interlocks may be used to prevent user access to hazardous areas, and to contain ejected parts and materials.
7. If the machine includes an independent tacho (velocity) feedback system, this should be cross-checked with the position feedback. For example, if the tacho indicates the axis is moving, but the position feedback doesn't, the axis motion must be stopped.
8. In the case of synchronised parallel motion systems (for example twin rail gantry drive systems), the relative positions of master and slave axes should be monitored. If the difference in their positions exceeds an expected limit, axis motion must be stopped.

For further advice, consult the appropriate machinery safety standards.

LSB resolution

It is important to set the LSB resolution of the RPI30 correctly. If the LSB resolution is set incorrectly, the axis may move for distances and at speeds that are not expected.

Direction sense

It is important to set the direction sense correctly. If it is set incorrectly, the machine will move in the opposite direction to that expected, and may accelerate until it reaches the axis limits. In the case of parallel twin rail drives, it is important that the direction sense of the slave axis is set to match the master axis. Failure to do this will cause opposite ends of the cross-member to move in opposite directions, possibly causing damage to the machine.

/Error signal monitoring

The RPI30 parallel interface continuously checks for internal errors and errors in the encoder system that may cause invalid position feedback signals, and signals a fault by asserting an /error line output. In the case of closed loop motion systems, for safe operation the status of this /error line must be monitored. If the /error line goes low, the position feedback signals may be incorrect and the axis of motion must be stopped.

Power supply out of range

The correct power supply voltage is 5 V ±0.25 V. Power supplies outside of this range may give unreliable operation or damage the RPI30 unit.

Position data integrity

If an error is signalled by the RPI30, then the RPI30 position data may be incorrect. The system must be reset and re-referenced before it is used for position feedback again.

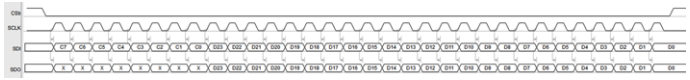
Appendix C

1 SPI programming guide

1.1 Timing

The SPI interface is a 32-bit slave, with the clock idling low, the data changing on the rising edge and latching on the falling edge (SPI mode CPOL = 0, CPHA = 0). CSb is taken low for the duration of the 32 bits. It consists of 8 command bits and 24 data bits shifted MSB first.

For a write operation the data to be written is loaded into the target register 10ns after the 32nd falling edge of the clock. The data clocked out on SDO is the contents of the target register before updating. For a read operation the data bits on SDI are ignored and the contents of the register clocked out on SDO. In both cases the first 8 bits clocked out on SDO are the command from the previous SPI operation. After power on, or a hard-reset command, they are all set to 1 (0xFF).



SPI link timing diagram.

	Min	Max	Units
SCLK frequency		10	MHz
SCLK high	50		ns
SCLK low	50		ns
CSb going low to rising edge SCLK	20		ns
Falling edge SCLK to CSb going high	20		ns
Setup of SDI before SCLK falling edge	10		ns
SDO valid after SCLK rising edge		40	ns

SPI link timing constraints.

1.2 Command makeup

The command byte defines whether the operation is a read or write and the register it is addressing. The data in the response to a write command is the previous contents of the addressed register. The address is made up of two parts, 4 bits for the block of registers and 3 bits for the register.

Bit	7	6 - 3	2 - 0
Function	Read – 0 / Write – 1	Block	Sub register

Command byte format.

2 Registers

2.1 Register map

Command	Value			Notes
	Block	Sub	R/W	
Version	0	0	R	FPGA version number
		1	R	PCB Revision number
		2	R	S/N Char 1-3
		3	R	S/N Char 4-6
		4	R	S/N Char 7-9
		5	R	S/N Char 10
ADC	1	0	R/W	Offset Sine
		1	R/W	Offset Cosine
		2	R/W	Scale Sine
		3	R/W	Scale Cosine
		4	R/W	ADC source
		5	R	ADC 1
		6	R	ADC 2 latched
		7	R	ADC 2 unlatched
Interpolator	2	0	R	Magnitude
		1	R	Angle Latched
		2	R	Angle unlatched
		3	R	Angle offset
Position	3	0	R	Low bytes
		1	R	High bytes
Output control	4	0		
		1	R/W	Parallel Bus Address
		2	R/W	Parallel Bus Direction
		3	R/W	Parallel Bus Resolution
		4	R/W	Parallel Bus Test output
		5	R/W	Enable bus settings change
Reset/ errors	5	0	R	Errors
		1	W	Reset Errors
		2	W	Soft reset FPGA
		3	W	Zero position
		4	W	Reset Angle offset
		5	W	Reset ADC min/max
		6	W	Hard reset FPGA
EEPROM	6	0	W	Read User calibration
		1	W	Write settings to EEPROM
		2	R/W	Enable write EEPROM
		3	R/W	Reserved Renishaw use
Lissajous correction status	8	0	R	Offset Sin
		1	R	Offset Cos
		2	R	AC Scale
		3	R	Phase scale 1
		4	R	Phase scale 2
		5	R	Velocity
		6	R	Status

Lissajous correction control	9	0	R/W	Enable
		1	R/W	Sampling length
		2	R/W	Min Quads
		3	R/W	Max Quads
		4	R/W	Offset filter length
		5	R/W	AC filter length
		6	R/W	Phase filter length
Data logger	10	0	R	Data
		1	R	Data
		2	R/W	Read address
		3	R/W	Sample rate divider
		4	R/W	Control
Reserved	15	0		Used by diagnostics interface – not implemented on SPI
		1		

Register map

2.2 Version (Block = 0)

2.2.1 FPGA version number (Sub = 0)

Read only register containing the FPGA version number. Each byte represents an integer interpreted as follows:

Bit	23 - 16	15 - 8	7 - 0
Function	Code type 0 - Release 1 - Beta 2 - Development	Main version number	Sub Version number

FPGA version number register definition.

2.2.2 PCB revision (Sub = 1)

Read only register containing the PCB revision in the least significant four bits. All other bits read as 0.

2.2.3 Serial number (Sub = 2 – 5)

Read only registers containing the serial number in the form of 10 ASCII characters. Table 3-3 shows the alignment of serial number characters to an array in C.

Register sub	23 - 16	15 - 8	7 - 0
2	C[2]	C[1]	C[0]
3	C[5]	C[4]	C[3]
4	C[7]	C[6]	C[2]
5	0		C[9]

Alignment of serial number characters within registers.

2.3 ADC (Block = 1)

2.3.1 Offset Sine/Cosine (Sub = 0, 1)

Read / write register containing a 16-bit signed integer offset which is added to the ADC value. The offset is set such that a 0V input gives less than 1mV residual offset. An initial factory calibrated value is loaded from EEPROM on power up, an additional user set can be stored in the EEPROM and loaded by load user EEPROM command or the values updated directly. Values are limited to between -2048 and +2047, values outside these limits will be set as +2047 for positive offsets or -2048 for negative ones. The raw ADC values are aligned to the top 12 bits of the offset register which give ≈ 20.3µV/LSB resolution and +/- 41.5mV range.

Bit	23 - 16	15 - 0
Function	Zeros	Offset value – signed integer

Offset register definition.

2.3.2 Gain Sine/Cosine (Sub = 2, 3)

Read / write register containing an 18-bit signed integer scale factor where 32768 is defined as a gain of 1. The scale factor is set such that a 1Vp-p input gives 100% signal strength. An initial factory calibrated value is loaded from EEPROM on power up, an additional user set can be stored in the EEPROM and loaded by load user EEPROM command or the values updated directly. The gain is limited to +/- 2 (+65535/-65536), values outside these limits will be set to +65535 for positive gains and -65536 for negative ones.

Bit	23 - 18	17 - 0
Function	Zeros	Gain value – signed integer

Gain register definition.

2.3.3 ADC source (Sub = 4)

Read / write register to set the source of the ADC data read from the ADC 1 and ADC 2 registers. The least significant four bits are used, data written to the other bits is ignored and read as zero.

Bit	23 - 4	3 - 0
Function	Zeros	ADC source

ADC source register definition.

ADC source	ADC 2	ADC 1	Notes
0	Sin Cal	Cos Cal	After calibration correction
1	Sin Raw	Cos Raw	Raw ADC data
2	Sin Raw Max	Sin Raw min	Min / max of raw data (reset by Reset ADC command)
3	Cos Raw max	Cos Raw min	
4	Sin Cal Max	Sin Cal min	Min / max of data after calibration (reset by Reset ADC command)
5	Cos Cal Max	Cos Cal min	
6	Zeros	Zeros	
7	Zeros	Zeros	
8	Sin	Cos	After offset/gain correction
9	Sin	Cos	After rotation
10	Sin	Cos	Corrected
11	Sin	Cos	Final corrected after saturation limits
12	Zeros	Zeros	
13	Zeros	Zeros	
14	Zeros	Zeros	
15	Zeros	Zeros	

ADC source locations.

The first eight sources are taken from the ADC front end and the second eight from the auto lissajous correction.

2.3.4 ADC values (Sub = 5, 6, 7)

Read only registers containing the ADC data as selected by the ADC source register. These are 16-bit signed integers. Scale factor is 500mV/2^13(≈0.061035mV/LSB), raw data will read ≈376mV for a 500mV input.

Bit	23 - 16	15 - 0
Function	Zeros	ADC value – signed integer

ADC value registers definition.

ADC 2 values are available in latched (6) and unlatched states (7). Reading the ADC 1 register (5) captures the current ADC 2 value in the latched ADC 2 register. This allows simultaneous reading of the two ADC channels.

2.4 Interpolator (Block = 2)

2.4.1 Magnitude (Sub = 0)

Read only register containing the 12-bit magnitude of the input signal. To convert to signal strength (100% = 1V p-p) divide by 20.47.

Bit	23 - 12	11 - 0
Function	Zeros	Magnitude – unsigned integer

Magnitude register definition.

2.4.2 Angle (Sub = 1, 2)

Read only registers containing the 12-bit angle in latched (1) and unlatched (2) state. To convert to degrees multiply by 360/4096.

Bit	23 - 12	11 - 0
Function	Zeros	Angle – unsigned integer

Angle register definition.

Reading the magnitude register (0) captures the current angle into the latched angle register (1). This allows the simultaneous reading of the magnitude and angle.

2.4.3 Angle offset (Sub = 3)

Read only register containing the angle offset stored when the position is zeroed. It can be reset to zero by the reset angle offset command.

Bit	23 - 12	11 - 0
Function	Zeros	Angle offset – unsigned integer

Angle offset register definition.

2.5 Position (Block = 3)

2.5.1 Position (Sub = 0, 1)

Read only registers containing the full internal 44-bit position sign extended to 48-bits in two registers, it isn't affected by the RPI30 emulation resolution setting. The high bytes register (1) is latched on reading the low bytes register (0), therefore to read the position read the low bytes first followed by the high bytes and concatenate the two. Scale factor is lissajous wavelength / 4096, which for a nominal 158nm lissajous is 38.574pm / LSB.

Bit	23 - 0
Definition	Least significant 24 bits of position – signed integer

Low bytes (Sub = 0) register definition.

Bit	23 - 20	19-0
Definition	Sign extended	Most significant 20 bits of position – signed integer

High bytes (Sub = 1) register definition.

2.6 Output control (Block = 4)

The output control registers provide the functionality of the switches on the RPI20, setting the address, direction and resolution of the parallel bus. Register bits set to 0 are equivalent to the RPI20 configuration switch being off, and 1 as the switch being on.

2.6.1 2.6.1 Parallel Bus Address (Sub = 1)

Read / write register containing the RPI30 address. It is loaded on power up from the EEPROM. In order to change the value, the Enable bus settings change command must be sent. Once the address

changes, an error is raised which is reported in the error register and on the parallel bus status as bus settings changed. Valid address range is 1-7, address 0 can be written but the bus will not be driven when address 0 is selected.

Bit	23 - 3	2 - 0
Definition	Don't care	Address

Parallel bus address register definition.

2.6.2 Parallel Bus Direction (Sub = 2)

Read / write register containing the parallel bus direction bit. It is loaded on power up from the EEPROM. In order to change the value, the Enable bus settings change command must be sent. Once the address changes, an error is raised which is reported in the error register and on the parallel bus status as bus settings changed.

Bit	23 - 1	0
Definition	Don't care	0 – Forward 1 – Reverse

Parallel bus direction register definition.

2.6.3 Parallel Bus Resolution (Sub = 3)

Read / write register containing the parallel bus resolution settings. It is loaded on power up from the EEPROM. In order to change the value, the Enable bus settings change command must be sent. Once the address changes, an error is raised which is reported in the error register and on the parallel bus status as bus settings changed.

Bit	23 - 2	1 - 0
Definition	Don't care	Resolution (approx. LSB for plane mirror) 00 – 38.6 pm 01 – 77.2 pm 10 – 154.4 pm 11 – 308.8 pm

Parallel bus resolution register definition.

2.6.4 Parallel Bus Test Output (Sub = 4)

Read / write register to set the parallel bus output when test information address is used. There is no need to use the enable bus settings change command and no error is generated when the register is changed.

Bit	23 - 3	2 - 0
Function	Don't care	Test output 000 – output 0xAAAAAAAAA 001 – output 0x555555555 010 – output 0x111111111 011 – output 0x222222222 100 – output 0x333333333 101 – output 0x444444444 110, 111 – output 0x000000000

Parallel bus test output register definition.

2.6.5 Enable bus settings change (Sub = 5)

In order to change the values in the address, direction or resolution registers 14 (0xE) must be written to this register. It must be written before each change. Reading the register returns the status.

Bit		23 - 4	3 - 0
Definition	Write	Don't care	14 (0xE)
	Read	Zeros	0 – disabled, 1 – enabled

Enable bus settings change register definition.

2.7 Reset / Errors (Block = 5)

2.7.1 Errors (Sub = 0)

Read only register containing the current errors and warnings. Warnings auto reset after 500ms, errors must be cleared by using a reset error command from one of the RPI30, diagnostics or SPI interfaces.

Bit	Type	Error	Notes
0	E	Encoder	External error passed on from encoder
1	E	Overspeed	Input has jumped 2 quadrants in one sample
2	E	Beam break	Signal magnitude < 12.5%
3	W	Beam saturation	Signal magnitude > 130%
4	W	Beam low	Signal magnitude < 25%
5	E	EEPROM CRC	CRC error occurred when reading settings from the EEPROM – can't be cleared
6	W	AC mismatch correction out of range	AC mismatch > +/-10%, correction limited to 10%
7	W	Offset correction out of range	Offset correction > +/-50mV, correction limited to 50mV
8	W	Phase correction out of range	Phase correction > +/-10%
9	E	Parallel bus settings changed	Address, resolution or direction settings for the parallel bus interface have changed
10-23		Not used	Zeros

Error register definition.

2.7.2 Reset errors (Sub = 1)

Writing anything to this register resets the current errors and warnings if the condition is no longer present. The errors and warnings can also be reset via the parallel bus.

2.7.3 Soft reset FPGA (Sub = 2)

Writing anything to this register causes the FPGA to reset the data path registers and parallel bus settings to the power on state.

- ADC offset and gain settings loaded from EEPROM
- Parallel bus settings loaded from EEPROM and the test output reset to 0xAAAAAAAAA
- Lissajous correction settings loaded from EEPROM
- Lissajous correction filters reset, offset to zero, gains to one, phase correction to 0.707

- Lissajous correction velocity calculations reset and updated from EEPROM
- Internal data logger stopped if running and settings reset to default
- Position counter zeroed, angle offset zeroed, ADC min/max reset, ADC source set to 0, write enables cleared, and errors cleared

The communications interfaces are not reset; therefore, the next SPI operation will return this command as the last command sent, and the diagnostics interface will not be interrupted.

2.7.4 Zero position (Sub = 4)

Writing anything to this register zero's the position by resetting the counter and capturing the current angle to be used as an offset (reported in the angle offset register) such that the output position is zero. The position can also be zeroed via the RPI30 interface.

2.7.5 Reset angle offset (Sub = 4)

Writing anything to this register resets the angle offset to 0.

2.7.6 Reset ADC min/max (Sub = 5)

Writing anything to this register resets the raw and corrected ADC min / max registers.

2.7.7 Hard reset FPGA (Sub = 6)

Writing 5395284 (0x525354) to this register causes the FPGA to generate an asynchronous reset, restoring it to the power on state.

2.8 EEPROM (Block = 6)

2.8.1 Read user calibration (Sub = 0)

Writing anything to this register causes the calibration offset and scale registers to be updated from the user calibration in the EEPROM.

2.8.2 Write settings to EEPROM (Sub = 1)

Write only register to initiate the settings being written to the EEPROM. The settings are split into three blocks;

- The lissajous correction control registers.
- The parallel bus settings – not including parallel bus Test Output register.
- User calibration – ADC offset and scale registers.

Set the relevant bit in the register to write that block to EEPROM, multiple bits can be set to update more than one block with a single command. The Enable write EEPROM command must be sent first and is cleared once this register is written to.

Bit	23 - 3	2	1	0
Definition	Not used	Lissajous correction settings	Bus settings	User calibration

Write settings to EEPROM register definition

The RPI30 and lissajous correction settings are read on power up to initialise the board (and when the reset FPGA command is sent). The user calibration can be read using the read user calibration command.

2.8.3 Enable write EEPROM (Sub = 2)

In order to write the settings to EEPROM write 14 (0xE) to this register. The enable is cleared once write settings to EEPROM register is written to. Reading the register returns its status.

Bit		23 - 4	3 - 0
Definition	Write	Don't care	14 (0xE)
	Read	Zeros	0 – disabled, 1 – enabled

Enable write EEPROM register definition.

2.9 Lissajous correction status (Block = 8)

2.9.1 Offset (Sub = 0, 1)

Read only registers containing the offsets applied to Sine and Cosine signals in the auto correction. Signed 18-bit integers, sign extended to 24-bit. 15.26µV/LSB (500mV/2^{15}).

2.9.2 AC scale (Sub = 2)

Read only register containing the gain applied to the Sine signal to correct for AC mismatch in the auto correction. Signed 18-bit integer, sign extended to 24-bit. 32768 = gain of 1.0.

2.9.3 Phase scale 1 (Sub = 3)

Read only register containing the gain applied to the Sine signal after rotation by 45 degrees to correct for phase in the auto correction. Signed 18-bit integer, sign extended to 24-bit. 32768 = gain of 1.0.

2.9.4 Phase scale 2 (Sub = 4)

Read only register containing the gain applied to the both Sine and Cosine signals after phase correction to correct for the gain introduced by the 45 degrees rotation in the auto correction. 100% signal on input to the auto correction gives 100% signal at the output. Signed 18-bit integer, sign extended to 24-bit. 32768 = gain of 1.0, nominal value is $1/\sqrt{2}$ (23170 = 0.7071).

2.9.5 Velocity (Sub = 5)

Read only register containing the number of quads traversed in the sampling period. 24-bit signed integer.

2.9.6 Status (Sub = 6)

Read only register containing the status of the auto correction for the last sample period.

Bit	23 - 10	3	2	1	0
Definition	Not used	Quad counter overflow	Overspeed warning (>1m/s for plane mirror)	Input velocity valid	Input magnitude valid

Lissajous correction status register definition.

The quad counter overflow bit is set when the number of quadrants traversed during the sampling period exceeds ±8388608 (2^{23}). When the bit is set the velocity register saturates and the counter stops until it is reset for the next sample period.

The overspeed warning bit is set if the calculated velocity is greater than 1m/s (based on 158nm / lissajous).

The input velocity valid bit is set when the quadrant count is greater than the minimum quadrants and less than the maximum quadrants set in the control registers and there was no overspeed event for the sample period.

The input magnitude valid bit is set if the lissajous was greater than 50% signal strength for the sample period.

For the correction coefficient filters to be updated both input valid bits need to have been set.

2.10 Lissajous correction control (Block = 9)

2.10.1 Enable (Sub = 0)

Read / write register containing the auto correction control bits.

Bit	23 - 7	6	5	4	3	2	1	0
Definition		Phase			AC mismatch		Offset	
	Not used	Bypass	Hold	Reset	Hold	Reset	Hold	Reset

Lissajous correction enable register definition.

Offset

Setting the reset bit disables the offset correction by setting the offset to 0, it overrides the hold bit.

Setting the hold bit disables the updating of the offset correction and the current value is used.

To run the offset correction both bits need to be cleared.

AC mismatch

Setting the reset bit disables the AC mismatch correction by setting the gain to 1, it overrides the hold bit.

Setting the hold bit disables the updating of the AC mismatch correction and the current value is used.

To run the AC mismatch correction both bits need to be cleared.

Phase

Setting the reset bit disables the phase correction by setting the effective gain to 1 but it still introduces a rotation of the lissajous, it overrides the hold bit. To avoid the rotation being introduced set the bypass bit.

Setting the hold bit disables the updating of the phase correction and the current value is used.

Setting the bypass bit takes the phase correction out of the signal path, the output of the offset and AC mismatch correction is fed directly into the interpolator. This removes the rotation added to calculate the phase correction.

To run the phase correction all three bits need to be cleared.

2.10.2 Sampling length (Sub = 1)

Read / write register containing the sampling length for the auto correction. It is a 24-bit unsigned integer in 1us increments.

2.10.3 Min quads (Sub = 2)

Read / write register containing the minimum number of quadrants the input must move within the sampling period. It is an 8-bit unsigned number. It shouldn't be a less than 4 quadrants (one lissajous).

Bit	23 - 8	7 - 0
Definition	Don't care	Unsigned integer

Minimum quads register definition

Combined with the sampling length, this determines the minimum velocity that the auto correction coefficients will be updated.

2.10.4 Max quads (Sub = 3)

Read / write register containing the maximum number of quadrants the input can move within the sampling period. It is a 24-bit unsigned integer. Combined with the sampling length, this determines the maximum input velocity that the auto correction coefficients will be updated.

2.10.5 Offset and AC filter length (Sub = 4, 5)

Read / write register containing the settings for the offset and AC mismatch filters.

Bit	23 - 3	1 - 0
Definition	Don't care	Filter length 00 – 8 bit 01 – 10 bit 10 – 12 bit 11 – 14 bit

Lissajous correction filter length registers definition.

The filters are n-bit exponential first order low pass filters with a filter coefficient given by Equation 1.

$$a = 1 - \frac{1}{2^n}$$

Equation 1 Exponential filter coefficient a for n-bit filter.

The time constant and -3dB frequency are calculated from the sample time (T), set in the sampling length register, and the filter coefficient (a) (Equation 2).

$$\tau = \frac{-T}{\ln a} \qquad F_c = \frac{1}{2\pi\tau}$$

Equation 2 Time constant and -3dB frequency of exponential filter.

2.10.6 Phase filter length (Sub = 6)

Future functionality.

2.11 Data logger (Block = 10)

The data logger collects 28672 samples of 6 bytes. The samples can be either ADC data selected from any of the monitor options, or position along with 8 error bits. Sample rate is set by the sample rate divider with 0 being 100MHz. Data should be read low bytes first then high bytes; the read address is auto incremented on reading the high bytes. The data logger registers are shared with the monitor interface so one interface can interfere with the other if they try and log at the same time.

2.11.1 Data (Sub = 0,1)

Data is split over two registers; low bytes (sub = 0) and high bytes (sub = 1).

Register	Byte	Position selected	ADC selected
0	0	40 bit position, signed integer	ADC1, signed integer
	1		
	2		ADC2, signed integer
1	0		
	1		ADC source
	2	Errors	Errors

Data logger data registers definitions.

ADC data and source are the same format as for direct reading of the ADC. The definition of the bits in the error byte are given in Table 3-27.

Bit	Error
0	Encoder error
1	Overspeed error
2	Beam break
3	Beam saturation
4	Beam low
5	AC mismatch correction out of range
6	Offset correction out of range
7	Phase correction out of range

Data logger error bits definition.

2.11.2 Read address (Sub = 2)

Valid read addresses are between 0 and 28671. The address is auto incremented on reading the high data bytes allowing the logged data to be read just by reading the data registers. The address automatically rolls over to 0 at the end or if the previous address was out of range.

2.11.3 Sample rate divider (Sub = 3)

The sample rate divider is a 24bit unsigned integer. The sample rate is calculated as follows

Sample rate = 100MHz/(sample rate divider + 1)

For 100MHz set divider to 0, for 50MHz set divider to 1 and so on.

2.11.4 Control (Sub = 4)

To start data logging write 1 to bit 0, bit 1 is then set when the logging finishes.

Bit 2 defines whether position or ADC data is collected. Bit 3 defines which ADC source register is used to define the ADC data collected.

Bit	23 - 4	3	2	1	0
Definition	N/A	R/W	R/W	R	W
	Not used	ADC source 0 – SPI control 1 – Monitor control	0 – Position 1 - ADC	Finished	Write 1 to start

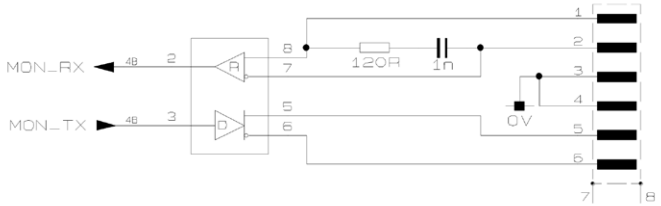
Data logger control register definition.

Appendix D

1 Diagnostics link

1.1 Physical

The diagnostics link is a full duplex RS422 serial interface. It utilises a UART running at 3M baud, 1 start bit, 8 data bits and 1 stop bit. Connection is via a 6-way PicoBlade connector on the side of the RPI30.



Diagnostics RS422 interface circuit diagram

1.2 Format

Accessing the registers uses the same command and data format as the SPI interface, with a header and footer to frame the packet. Because the request has to be completely received and processed before sending the response, the data returned is from after the write operation rather than before as in the SPI case. A request can be received during transmission of a streaming or RAM download packet, in that case the response is transmitted as soon as transmission of the current packet is complete. The check sum byte is the negative of the sum of all the previous bytes such that the sum of all 6 bytes is 0.

Byte	Value	Notes
0	0xAA	Header
1	Command	Command byte
2	Data byte 2	Bits 23 – 16
3	Data byte 1	Bits 8 – 15
4	Data byte 0	Bits 7 – 0
5	Check sum	Negative of the sum of the previous bytes

Register access packet format.

If the received packet has an incorrect checksum then no response is sent. The receive state machine times out 5ms after detecting the header byte in the case of an incomplete packet, and resets to waiting for the header byte again.

2 Registers

All the registers are defined in the SPI interface specification, other than an extra two registers which are only accessible via the diagnostics interface.

2.1 Differences to SPI interface

2.1.1 ADC source and data

The ADC source and value registers are a separate set from the SPI ones, allowing the diagnostics interface to monitor different ADC points from the controller.

2.1.2 Reset

Only reset errors, zero position and reset ADC min/max options are available. The reset ADC min/max resets the diagnostics interface registers and not the SPI interface registers.

2.2 Diagnostics (Block = 15)

2.2.1 Streaming enable (Sub = 0)

Reading registers individually is a relatively slow process, in order to collect data at a faster rate a streaming mode is available. The format of the streamed data is given in section 4. Set bit 0 to start streaming and clear to stop. The stream rate is set in bits 8 and 9.

Bit	23-10	9-8	7-1	0
Function	Zeros	Streaming rate 00 – 5kHz 01 – 2kHz 10 – 1kHz 11 – 500Hz	Zeros	Streaming enabled

Streaming enable register definition.

2.2.2 Download RAM (sub = 1))

To speed up reading of the datalogger RAM it can be read as packets consisting of 8 samples. The download is initiated by setting bit 0, the number of packets in bits 1 and 2, and the start address in bits 8-19. The entire contents of the RAM can be downloaded in one go, but this can be unreliable when used with a RS422 to USB adapter, when the USB bus is busy the converter buffer overruns, losing data.

The valid range for start address is 0 to 3583 for single packet downloads, 0 to 3551 for 32 packet downloads and 0 for all packet downloads. If an out of range address is set it is internally set to the maximum value for the number of packets.

Bit	23 - 10	19 - 8	7 - 3	2 - 1	0
Function	Zeros	Start address 0 - 3583	Zeros	Number of packets 00 – all (3584) 01 – 1 10 – 32 11 – all	Start download

Download RAM register definition.

3 Streaming data

3.1 Packet format

The streaming data packet is 34 bytes long and transmitted at the rate defined in the streaming enable register. Values are transmitted least significant byte first. Scale factors and definitions are the same as for their equivalent registers.

Byte	Function	Type	Notes
0	Header	0xAB	
1	ADC 1 byte 0	16-bit signed integer	Source set in the diagnostics ADC source register
2	ADC 1 byte 1		
3	ADC 2 byte 0	16-bit signed integer	
4	ADC 2 byte 1		
5	Position byte 0	40-bit signed integer	Full resolution position
6	Position byte 1		
7	Position byte 2		
8	Position byte 3		
9	Position byte 4		
10	Offset 1 byte 0	24-bit signed integer	Correction – offset for Sin
11	Offset 1 byte 1		
12	Offset 1 byte 2		
13	Offset 2 byte 0	24-bit signed integer	Correction – offset for Cos
14	Offset 2 byte 1		
15	Offset 2 byte 2		
16	AC byte 0	24-bit signed integer	Correction – AC mismatch scale factor
17	AC byte 1		
18	AC byte 2		
19	Phase 1 byte 0	24-bit signed integer	Correction – phase scale factor
20	Phase 1 byte 1		
21	Phase 1 byte 2		
22	Phase 2 byte 0	24-bit signed integer	Correction – phase rotation correction scale factor
23	Phase 2 byte 1		
24	Phase 2 byte 2		
25	Velocity byte 0	24-bit signed integer	Velocity
26	Velocity byte 1		
27	Velocity byte 2		
28	Status	Flags	Correction status byte
29	SS byte 0	16-bit unsigned integer	Signal strength (magnitude)
30	SS byte 1		
31	Errors byte 0	Flags	Errors
32	Errors byte 1		
33	Footer	Check sum	Negative of the sum of all preceding bytes

Streaming data packet format

4 Download datalogger RAM

The RAM download packet is 52 bytes long, consisting of 8 48-bit samples and the start address. The data is transmitted least significant byte first. Data format is the same as the equivalent data logger data registers.

Byte	Function	Type	Notes
0	Header	0xAC	
1	Address byte 0	16-bit signed integer	Address of the block of data
2	Address byte 1		
3	Data 0 byte 0	48-bit sample	1st sample in block starting at address at the start of the packet. Contents depends on whether ADC data or position data was logged.
4	Data 0 byte 1		
5	Data 0 byte 2		
6	Data 0 byte 3		
7	Data 0 byte 4		
8	Data 0 byte 5		
9 - 14	Data 1	48-bit sample	2nd sample
15 - 20	Data 2	48-bit sample	3rd sample
21 - 26	Data 3	48-bit sample	4th sample
27 - 32	Data 4	48-bit sample	5th sample
33 - 38	Data 5	48-bit sample	6th sample
34 - 44	Data 6	48-bit sample	7th sample
45 - 50	Data 7	48-bit sample	8th sample
51	Footer	48-bit sample	Negative of the sum of all preceding bytes

RAM download packet format.

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